REMARKS

The Official Action mailed October 24, 2002 has been received and its contents carefully noted. Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on July 26, 2002; July 15, 2002; June 3, 2002; and July 30, 2001.

Claims 2-6, 8-12, and 14-42 are pending in the present application of which claims 3, 9, 15, 20, 25, 29, 35 and 40 are independent. Claims 3, 9, and 15 have been amended herewith. It is noted that the Official Action Summary recognizes that claims 20-42 are pending, however, the body of the Official Action makes no reference to or rejection of these claims. Therefore, a further substantive Official Action clarifying the status of these claims is believed to be appropriate in response to this amendment and is respectfully requested. For the reasons set forth in detail below, these claims are believed to be in condition for allowance.

Paragraph 3 of the Office Action rejects claims 1-19 as obvious based on the combination of U.S. Patent 6,236,064 to Mase and U.S. Patent 5,903,249 to Koyama. Paragraph 4 of the Office Action further rejects claims 13-19 as obvious based on the combination of Mase, Koyama, and U.S. Patent 5,581,092 to Takemura.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Independent claims 3, 9, and 15 have been amended herewith to recite that a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween. It is respectfully submitted that none of Mase, Koyama or Takemura disclose or suggest this feature of the present invention. Since the prior art, taken alone or in combination, fails to disclose or suggest all the claim limitations, it is respectfully submitted that a *prima facie* case of obviousness cannot be maintained and favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

3. (Twice Amended) A method of manufacturing a semiconductor device:

the semiconductor device comprising: at least two p-channel thin film transistors in a pixel portion,

each of the two p-channel thin film transistors in the pixel portion fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V[.], and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.

9. (Twice Amended) A method of manufacturing a display device, said display device comprising:

a pixel portion and a driving circuit portion;

at least two p-channel thin film transistors being formed in the pixel portion;

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V[.], and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.

15. (Twice Amended) A method of manufacturing a semiconductor device, said semiconductor device comprising:

at least a first p-channel thin film transistor and a second p-channel thin film transistor in a pixel portion;

a transmission gate including a CMOS circuit, said CMOS circuit including at least an n-channel thin film transistor and a third p-channel thin film transistor;

each of the first, second and third p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the first and second p-channel thin film transistors are connected in series,

wherein an off current from each of the first, second and third p-channel thin film transistors is less than 10^{-12} A where a voltage of the drain region is 1V[.], and

wherein a pixel electrode is connected to a data line without any n-channel thin film transistor connected therebetween.